REMARKS

Claims 1-23 are pending in the present application.

Claims 1-23 stand rejected under 35 U.S.C. §102(e) as being anticipated by Larson et al. (U.S. Patent Publication 20030033464) (hereinafter "Larson"). Applicant respectfully traverses this rejection.

Applicant's remarks and arguments made in the previous response dated February 17, 2006 are maintained herein. In addition, Applicant further submits the following remarks in response to the Examiner's Response to Arguments. More particularly, the Examiner asserts on page 11, that "It is clear that claim 1 does not require "intermediate states or mapping hot-swap states" and that "hot-swap states must be mapped to intermediate states."" Applicant respectfully disagrees with the Examiner's assessment of what claim 1 requires.

Applicant's claim recites in pertinent part

> "**mapping said hot-swap state onto an intermediate state** by searching a **common library associated with said CPCI node card and a management software** for said CPCI node card; and
>
> **mapping said intermediate state onto a first management state of said management software** and **a second management state of said management software**;
>
> wherein said management software requires both said first and second management states to manage said CPCI node card." (Emphasis added)

From the foregoing, Applicant submits claim 1 does, in fact, require 2 mapping steps: mapping a hot swap state onto an intermediate state, and mapping the intermediate state onto a first and a second management state of management software. Applicant

fails to understand why the Examiner would believe the there is no mapping required by the claim.

In addition, the Examiner appears to be interpreting Larson's 18 status input lines as some 18 different hot-swap statuses and thus some "common library" of hot-swap states within the FPGA. Applicant disagrees with this interpretation. More particularly, Applicant points out the 18 input lines are just that; 18 individual wires/lines each with a single input that is associated with a single device. Further, Applicant notes that in the electrical arts, especially as used in board and circuit interconnections, it is well known that a line generally refers to a single wire or single signal path, and NOT that "it is clear that each swap line includes a plurality of hot swap statuses (states) inputs" as the Examiner has suggested. Applicant believes the Examiner is attempting to infer a definition of the input lines and the operation of the FPGA of Larson based upon outside references. However, Applicant submits the inferences are being made by the Examiner are unfounded. Any inferences made as to whether the FPGA has some "library" is purely speculation.

Larson does not teach any such input line definition as discussed in [0036] and [0061-0064]. Moreover, Applicant submits the hot-swap states discussed and shown in the HIP1011 document cited by the Examiner are states derived from a number of signal inputs including the HEALTHY#, ENUM#, PCI_RST#, and BDSEL# signals. The HEALTHY# and BDSEL# signals are shown in Larson. In fact, Larson never mentions the configuration of the hot-swap status input lines in any other way than there are 18 hot-swap status input lines to the FPGA. Applicant submits Larson teaches the hot-swap status input signals are used by the SMC 300E (the processor) to determine the hot-swap status of a number of various components the hot swap status input lines 522B.

In regard to the Examiner taking the liberty of defining Applicant's claimed common library to mean the common library provided by the FPGA is the 18 hot swap statuses provided by the 18 hot swap input lines. Applicant respectfully disagrees with the Examiner's analogy. More particularly, Applicant has already established that Larson

does not provide such 18 hot swap statuses. To the contrary, Larson teaches 18 hot-swap status input lines. Applicant believes the Examiner is mis-interpreting the language. Applicant finds it hard to believe that the Examiner is asserting that the FPGA provides a library of hot swap statuses. This is not taught or suggested in Larson. In addition, Applicant notes that Larson explicitly teaches that the SMC 300E determines the hot-swap state. Larson teaches merely that an interrupt is sent to SMC 300E when a card is removed or installed. Applicant submits the interrupts are generated by the FPGA, but this is also speculation, as Larson is unclear who generates the interrupts.

Further, Applicant further notes that just because software running on SMC 300E may determine the hot-swap status, it does not mean there is mapping as recited in Applicant's claims.

More particularly, Applicant submits Larson **does not teach or disclose** "**mapping said hot-swap state onto an intermediate state by searching a common library associated with said CPCI node card and a management software for said CPCI node card**, as recited in Applicant's claim 1. Applicant also submits Larson **does not teach or disclose** "**mapping said intermediate state onto a first management state of said management software and a second management state of said management software**." Applicant further submits Larson **does not teach or disclose** "wherein said management software requires both said first and second management states to manage said CPCI node card," as recited in Applicant's claim 1. (Emphasis added)

For the foregoing reasons, Applicant respectfully submits claim 1 along with its dependent claims, patentably distinguishes over Larson.

Claim 10 includes limitations that are similar to limitations recited in claim 1. Accordingly, Applicant submits claim 10, along with its dependent claims, patentably distinguishes over Larson for at least the reasons given above.

Applicant's claim 7 recites a method comprising in pertinent part

"mapping said PICMG hot-swap state onto an intermediate state by searching a common library associated with said CPCI node card and a management software for said CPCI node card; and

mapping said intermediate state onto a Telecommunication Management Network (TMN) plug-in unit state of said management software;

wherein said management software requires said TMN plug-in unit state to manage said CPCI node card." (Emphasis added)

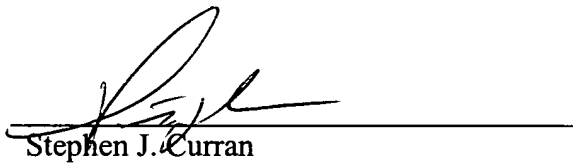
As described above, Applicant submits these features are not taught by Larson. Thus, Applicant respectfully submits claim 7 along with its dependent claims, patentably distinguishes over Larson, for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/6000-10201/SJC.

Respectfully submitted,



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